CLAIMS

1. An amplifier circuit comprising:

a first input terminal;

a first output terminal;

a first complementary metal-oxide-semiconductor (CMOS) inverter coupled between the first input terminal and the first output terminal;

a first bias circuit for applying linear biasing to an input of the first CMOS inverter, the first bias circuit being coupled between an output of the first CMOS inverter and the input of the first CMOS inverter.

2. The amplifier circuit of Claim 1, wherein the first input terminal is coupled to the input of the first CMOS inverter by a first capacitor, and

wherein the first output terminal is coupled to the output of the first CMOS inverter by a second capacitor.

3. The amplifier circuit of Claim 1, wherein the first CMOS inverter comprises:

a p-type metal-oxide-semiconductor (PMOS) transistor; and

an n-type metal-oxide-semiconductor (NMOS) transistor,

wherein the PMOS transistor and the NMOS transistor are serially connected between an upper supply voltage and a lower supply voltage,

wherein a gate of the PMOS transistor and a gate of the NMOS transistor are connected to the input of the first CMOS inverter, and

wherein a drain of the PMOS transistor and a drain of the NMOS transistor are connected to the output of the first CMOS inverter.

4. The amplifier circuit of Claim 3, wherein the first bias circuit comprises an operational amplifier, wherein a non-inverting input of the op-amp is coupled to the output of the first CMOS inverter, wherein an output of the op-amp is coupled to the input of the first CMOS inverter, and wherein an inverting input of the op-amp is coupled to receive a reference voltage, the reference voltage being between the first supply voltage and the second supply voltage, the first supply voltage being greater than the second supply voltage.

5. The amplifier circuit of Claim 4, wherein the reference voltage is halfway between the first supply voltage and the second supply voltage.

6. The amplifier circuit of Claim 4, wherein the non-inverting input of the op-amp is coupled to the output of the first CMOS inverter by a first resistor, and

wherein the output of the op-amp is coupled to the input of the first CMOS inverter by a second resistor.

7. The amplifier circuit of Claim 6, wherein the non-inverting input of the op-amp is coupled to the second supply voltage by a first capacitor, and

wherein the output of the op-amp is coupled to the second supply voltage by a second capacitor.

8. The amplifier circuit of Claim 1, further comprising an amplifier stage coupled to the first output terminal.

9. The amplifier circuit of Claim 8, wherein the amplifier stage comprises:

a second input terminal coupled to the first output terminal;

a second output terminal;

a second CMOS inverter coupled between the second input terminal and the second output terminal; and

a second bias circuit for applying linear biasing to an input of the second CMOS inverter, the second bias circuit being coupled between an output of the second CMOS inverter and the input of the second CMOS inverter.

10. A method for operating a high frequency amplifier, the method comprising:

providing a complementary metal-oxide-semiconductor (CMOS) inverter having an inverter input and an inverter output;

applying linear biasing to the inverter input; and

supplying an alternating current (AC) signal to the inverter input to generate an amplified AC signal.

11. The method of Claim 10, wherein supplying linear biasing to the inverter input comprises:

monitoring a direct current (DC) operating voltage at the inverter output; and

supplying a DC bias voltage to the inverter input to drive the DC operating voltage to a reference voltage.

12. The method of Claim 11, wherein monitoring the DC operating voltage comprises providing the DC operating voltage to a non-inverting input of an operational amplifier (op-amp), and

wherein supplying the DC bias voltage comprises providing the reference voltage to an inverting input of the op-amp and providing an op-amp output voltage to the inverter input.

13. The method of Claim 12, wherein providing the DC operating voltage to the non-inverting input of the op-amp comprises coupling the inverter output to the non-inverting input of the op-amp via a first resistor, and

wherein providing the op-amp output voltage to the inverter input comprises coupling an output of the op-amp to the inverter input via a second resistor.

14. The method of Claim 13, wherein the CMOS inverter comprises a PMOS transistor and an NMOS transistor serially connected between an upper supply voltage and a lower supply voltage, and

wherein the reference voltage is halfway between the upper supply voltage and the lower supply voltage.

15. The method of Claim 14, wherein the op-amp output voltage to the inverter input further comprises coupling the output of the op-amp to the lower supply voltage via a first capacitor, and

wherein providing the DC operating voltage to the non-inverting input of the op-amp further comprises coupling the non-inverting input of the op-amp to the lower supply voltage via a second capacitor.

16. The method of Claim 14, wherein supplying the AC signal to the inverter input comprises:

receiving a high frequency input signal; and

filtering out DC components from the high frequency input signal to generate the AC signal.

17. The method of Claim 16, further comprising:

filtering out DC components from the amplified AC signal to generate an output AC signal; and

supplying the output AC signal to an amplifier gain stage.

18. A high frequency amplifier comprising:

a complementary metal-oxide-semiconductor (CMOS) inverter; and

means for regulating a DC bias voltage at an input of the CMOS inverter to force a DC operating voltage at an output of the CMOS inverter to a reference voltage.

19. The high frequency amplifier of Claim 18, wherein the CMOS inverter comprises:

a p-type metal-oxide-semiconductor (PMOS) transistor, wherein a gate of the PMOS transistor is connected to the input of the CMOS inverter, and wherein a drain of the PMOS transistor is connected to the output of the CMOS inverter; and

an n-type metal-oxide-semiconductor (NMOS) transistor, wherein a gate of the NMOS transistor is connected to the input of the CMOS inverter, wherein a drain of the NMOS transistor is connected to the output of the CMOS inverter, and wherein the PMOS transistor and the NMOS transistor are serially coupled between an upper supply voltage and a lower supply voltage, the reference voltage being between the upper supply voltage and the lower supply voltage.

20. The high frequency amplifier of Claim 19, wherein the reference voltage is halfway between the upper supply voltage and the lower supply voltage.

21. The high frequency amplifier of Claim 19, wherein the means for regulating the DC bias voltage comprises:

a voltage generator for generating the reference voltage; and

an operation amplifier (op-amp) comprising:

a non-inverting input coupled to the output of the CMOS inverter via a first resistor;

an inverting input coupled to receive the reference voltage from the voltage generator; and

an op-amp output coupled to the input of the CMOS inverter via a second resistor.

22. The high frequency amplifier of Claim 21, wherein the means for regulating the DC bias voltage further comprises:

a first capacitor coupled between the non-inverting input and the lower supply voltage; and

a second capacitor coupled between the op-amp output and the lower supply voltage.

23. An amplification circuit comprising:

a complementary metal-oxide-semiconductor (CMOS) inverter coupled between an upper supply voltage and a lower supply voltage; and

an operational amplifier (op-amp) comprising:

a non-inverting input coupled to an output of the CMOS inverter;

an inverting input coupled to receive a reference voltage, the reference voltage being between the upper supply voltage and the lower supply voltage; and

an output coupled to an input of the CMOS inverter.

24. The amplification circuit of Claim 23, wherein the non-inverting input is coupled to the output of the CMOS inverter by a first resistor, and

wherein the output of the op-amp is coupled to the input of the CMOS inverter by a second resistor.

25. The amplification circuit of Claim 24, wherein the non-inverting input of the op-amp is coupled to the lower supply voltage by a first capacitor, and

wherein the output of the op-amp is coupled to the lower supply voltage by a second capacitor.

26. The amplification circuit of Claim 25, further comprising:

an input terminal coupled to the input of the CMOS inverter by a third capacitor; and

an output terminal coupled to the output of the CMOS inverter by a fourth capacitor.